A Low Power Relaxation Oscillator with Process Insensitive Auto-Calibration Scheme

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***Abstract*—In this paper, we present an auto-calibrated process insensitive relaxation oscillator. A process sensitivity of 1.36% is achieved by automatically sensing the output clock frequency spread and alternatively adjusting the capacitor-used for charging and discharging. In addition, a time to digital converter is adopted for tuning the compensating capacitor. Moreover, the proposed oscillator with on-chip calibration scheme, implemented by UMC 0.18μm 1P6M standard process, is validated by our reported extensive post-layout simulation results. A frequency of 32.7 kHz can be generated by operating the system under 1V supply voltage.**

I. INTRODUCTION

On-chip clock generator is widely-exploited in low power portable applications such as wireless sensor networks (WSN), etc. [1]. Different from most circuit building blocks, the clock is always active and consumes a large amount of energy, making low-power clock design essential in emerging wireless applications. Meanwhile, in a wide range of radio frequency identification (RFID) related applications [2], small inter-die variation is a stringent requirement for the clock generator.

To design a uniform clock across different process conditions, Lim Joonhyung *et al.* proposed an auto calibration engine that utilizes a digital block to control bits of R/C [3], it exhibits a process variation of 1.52% among 200 samples. A frequency reference reported by G. D. Vita *et al.* utilizes the electron mobility which is intrinsically stable to mitigate the process variation induced frequency drifts [4]. Nevertheless, the process variation without calibration achieve the reported 11.85% inter-die spread. In [5], a process immune oscillator was reported by dedicatedly compensating the comparator's non-idealities caused by its offset voltage and delay time, together with digital calibration, the achieved inter-die spread is still as large as 2.3%.

In this paper, we present a relaxation oscillator with inter-die frequency variation 1.36%. Using the proposed auto-calibration methodology, the need of the aforesaid dedicated calibration is replaced by an auto-calibration scheme, leading to faster calibration speed, thus lower cost while higher accuracy. The remaining of this paper is organized as follows. Section II describes the operation principle and the implementation of the auto-calibration scheme. Section III presents the error induced by process variation and design consideration of the on-chip calibration. Section IV presents the simulation results and the conclusion is drawn in Section V.

II. OPERATION PRINCIPLE

Figure 1 shows the block diagram of the proposed auto-calibrated clock generator. It consists of a reference generator, a relaxation oscillator, a time to digital converter which can be turned off after calibration and a compensation capacitor array. The time to digital converter is applied to sense the frequency spread induced by process variation. Concretely, the reference provides a bias current I_{bias} for the relaxation oscillator to charge/discharge the capacitor and a current to keep the comparator operating. Meanwhile, it generates reference voltages V_{bias1} for the switch capacitor circuitry and V_{bias2} for comparison during auto-calibration phase, both of which are detailed in the following section.

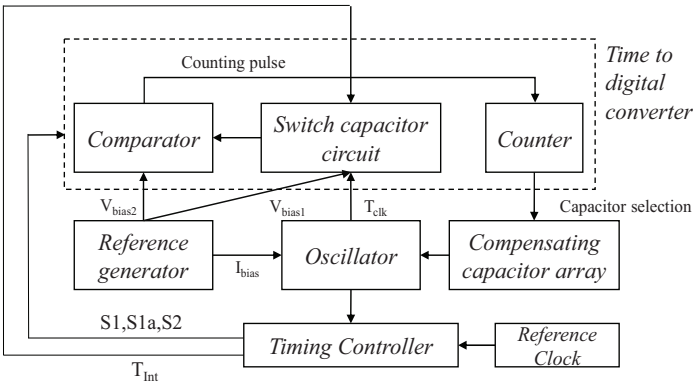

Fig. 1. Proposed oscillator architecture with auto-calibration.

As shown in Fig.1, during operation the output frequency of the raw oscillator is injected into the switch capacitor circuitry and determines the voltage of the capacitor which is connected to the input of the comparator, which then drives a digital counter. The counter output changes the compensating capacitor array and adjusts the oscillator frequency accordingly. After several cycles, the oscillator's frequency is maintained uniform with respect to a reference frequency, which behaves like a modified but more relaxed phase-locked loop. To minimize the error contribution from the compensation circuit, an on-chip process insensitive calibration circuit is utilized.

A Reference Generator

The schematic of the reference generator is presented in Fig. 2, where the transistors M_1 and M_2 operate at the subthreshold region. M_3 and M_4 operate as the current mirror pair. Moreover, a cascode current mirror, composed of M_{10}, M_{11}, M_{12}, M_{13} is introduced to make the gate voltages of M_{10}, M_{12} insensitive to the variation of bias voltages V_{bias1} and V_{bias2} (caused by the charge injection of switch capacitor circuits). In addition, M_5, M_6, M_7 form a typical start-up circuit featuring compact area. Here the bias current is equal to:

$$I_{bias} = \frac{mV_T \ln(\frac{K_{M1}K_{M4}}{K_{M3}K_{M2}})}{R1}, \quad (1)$$

where $V_T = kT/q$ is a process-independent thermal voltage that is proportion to the absolute temperature, m is a process related parameter and K_{M1}, K_{M2}, K_{M3}, K_{M4} are W/L ratios of the corresponding transistors. Typically, the value of V_T at room temperature is about 26 mV. Such a small current I_{bias} can be achieved by increasing R_1. According to Eq. (1), the bias current is determined by the transistors' W/L ratio, the absolute temperature and R_1. Alternatively, we can replace the resistor R_1 with a transistor working at the linear region in order to significantly decrease the silicon area. However, this is at the expense of system stability and robustness to the process variation.

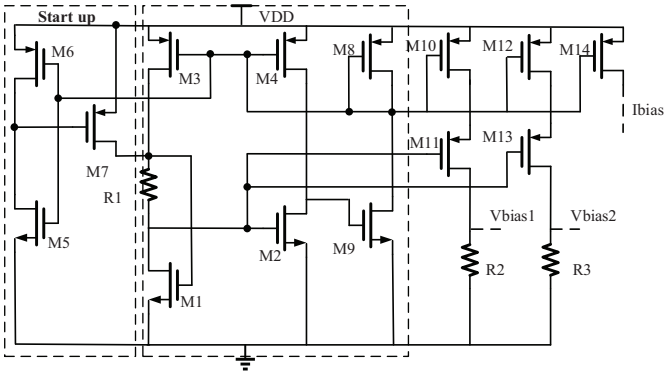

Fig. 2. Schematic of the proposed reference generator.

B Oscillator

In order to further reduce the power consumption, a Schmitt trigger is adopted as a comparator. The schematic is shown in Fig. 3, it consists of two current source, charging capacitor C_r, compensating capacitor array C_c, a Schmitt trigger [6] and an inverter acting as buffer. If the charging and discharging currents are equal, the clock cycle can be simplified as:

$$T_{clk} = \frac{2(V_{thh} - V_{thl})(C_r + C_c)}{I_{charge}}, \quad (2)$$

where V_{thh} and V_{thl} are the thresholds of Schmitt trigger, C_r is the charging capacitor, C_c is compensating capacitor with the initial value of 0 and I_{charge} is the charging current mirrored from I_{bias}. The delay caused by the Schmitt trigger and inverter within 10 ns is negligible due to the long clock period of nearly 31μs.

C Time to Digital Converter

Figure 4 illustrates the schematic of the adopted time to digital converter, the control signals are all generated by the original clock except for the control signal M_{23}. *Clk* and *Clk'* are two complementary clock signals generated by a non-overlapped circuits which are not shown. M_{21}, M_{22}, C_1 are connected to form a typical switch capacitor circuits. Both of C_1 and C_2 are initialized to zero at first, $V_{c2}(0)$ increase half of V_{bias1} after the first clock cycle, then $V_{c2}(1)$ increase half of $V_{c2}(0)$ after the second period and $V_{c2}(n)$ equals to $1.5V_{c2}(n-1)$ afterwards. The integration time of C_2 is controlled by the switch M_{23}, V_{bias1} is the above-mentioned reference voltage. V_{bias2} is set to between $0.5V_{bias1}$ and $0.75V_{bias1}$.

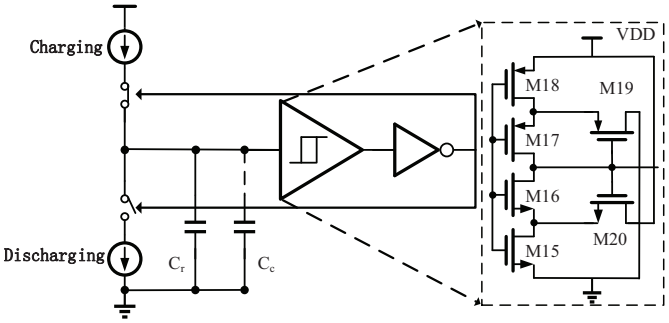

Fig. 3. Schematic of the proposed relaxation oscillator.

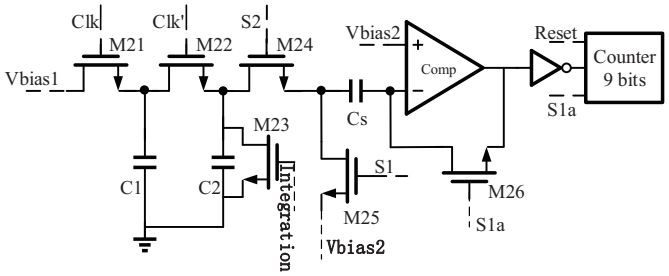

Fig. 4. The implementation of the adopted time to digital converter.

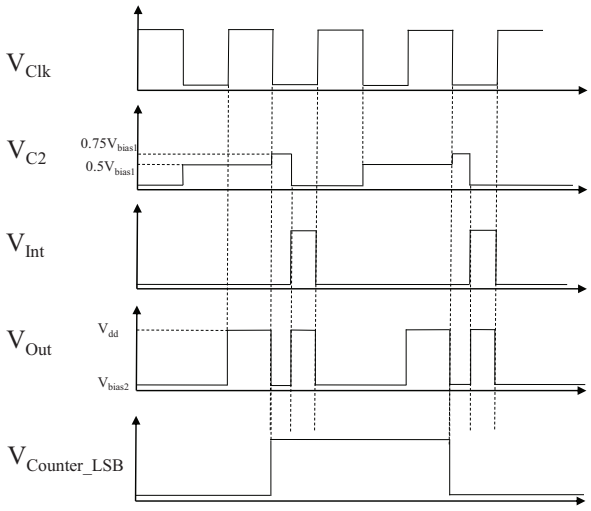

Fig. 5. Operation Waveform of the proposed time to digital converter.

The calibration process behave as shown in Fig.5: with an integration pulse injected, the switch M_{23} turns on and off periodically. Before M_{23} is on, the voltage V_{c2} increases to $0.5V_{bias}$ after the first cycle. The output of comparator will not change its logic during this time. After one and a half cycle, V_{c2} rises up to $0.75V_{bias}$. Then the comparator's output logical level alters and generates a falling edge signal to drive the counter which controls the clock signal T_{clk}. Afterwards, the switch M_{23} turns on to make V_{c2} change to zero and one calibration course is completed. The comparator generate a falling edge when V_{c2} reaches $0.75V_{bias}$ which indicate that if $1.5T_{clk}$ are smaller than the time T_{int} set by switch M_{23}, T_{clk} is unstable until $1.5T_{clk}$ is no less than T_{int}. Since T_{int} is set to be larger than $1.5T_{clk}$ initially, T_{clk} continually increase to guarantee $1.5T_{clk}$ is close to T_{int}. The increasing time step of T_{clk} is nearly 0.2% of T_{clk}, neglecting the time step error, we obtain:

$$\frac{3}{2}T_{clk} + t_d \approx T_{\text{int}} \tag{3}$$

where T_{clk} is the clock cycle, t_d is the delay time of the comparator, T_{int} is the integration time determined by the external pulse. The reference period can be expressed as:

$$T_{ref} \approx \frac{2}{3}(T_{\text{int}} - t_d) \pm t_{\log ical}, \tag{4}$$

where $t_{logical}$ is the time interval between the high and low marginally logical output level of the comparator. M_{24}, M_{25}, M_{26} form a typical offset cancellation scheme and C_s is the sample capacitor which is designed to be $500fF$ in this design taking consideration of the speed, the noise induced by charge injection and the chip area.

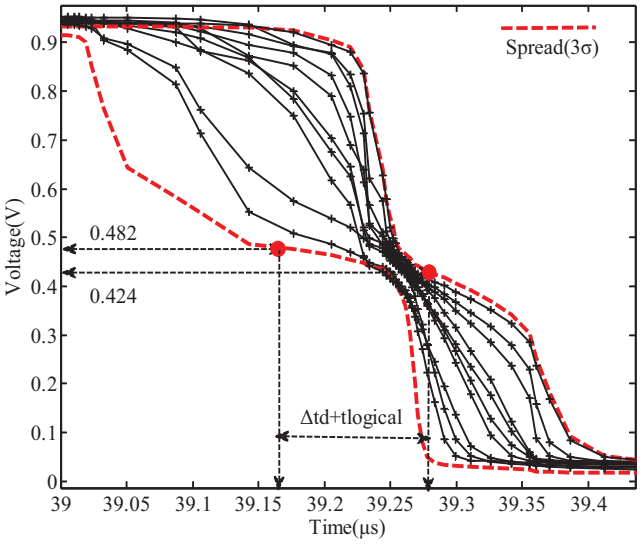

Fig. 6. Time interval which consist of Δt_{delay} and $t_{logical}$.

III. Oscillator Process Variation and On-chip Calibration

A Oscillator Process Variation

Combining Eq. (1) and (2), the final clock period T_{clk} is written as follows:

$$T_{clk} = \frac{2R_1C_r(V_{thh} - V_{thl})q}{kT \ln m}, \tag{5}$$

Meanwhile, m represents the ratio of $K_{M1}K_{M4}$ over $K_{M2}K_{M3}$. Considering the process variation and assuming V_{th}=V_{thh}-V_{thl}, Eq. (5) is rewritten as:

$$\begin{aligned} T_{clk} + \Delta T_{clk} &\approx T_{clk}(1+\frac{\Delta R_1}{R_1})(1+\frac{\Delta C_r}{C_r})(1+\frac{\Delta V_{th}}{V_{th}}) \\ &\approx T_{clk}(1+\delta_{R_1})(1+\delta_{C_r})(1+\delta_{V_{th}}), \end{aligned} \tag{6}$$

Here we neglect the mismatching errors of transistors K_{M1}, K_{M2}, K_{M3}, K_{M4}. It can be seen that the main error sources comes from the resistor R_1, the capacitor C_r and the threshold voltage V_{th} of Schmitt trigger. In this work implemented by UMC 0.18μm 1P6M standard process, the variation (3σ) of R_1, C_r, V_{th} are ±20%, ±20% and ±20%, respectively. In the worst-case scenario, the whole error induced by process variation is evaluated to be approximately ±60%.

B On-chip Calibration

The reliability of time to digital converter depends on the superior matching of C_1, C_2, V_{bias1} and V_{bias2}. Those two voltages depend on the ratio of R_2 over R_3, which can be guaranteed through common-used layout skills (e.g. common centroid). Considering the comparator's delay time variation induced by process spread, Eq. (4) can be rewritten as:

$$\begin{aligned} T_{ref} &\approx \frac{2}{3}[T_{\text{int}} - (t_d \pm \Delta t_d)] \pm t_{\log ical} \\ &\approx \frac{2}{3}(T_{\text{int}} - t_d) \pm [(\Delta t_d \pm t_{\log ical}) - \frac{1}{3}\Delta t_d], \end{aligned} \tag{7}$$

If 0.7V and 0.3V of are regarded as the high and low level for the output of the inverter before the counter in Fig. 4, its input voltage which is also the output of the comparator ranges from 0 to 424.5mV and 482.3mV to 1V respectively in the worst case scenario, according to 100 runs of *Monte Carlo* simulation results. By appropriately sizing of the transistors in the comparator, the time interval between the two output threshold voltages, corresponding to the second part of Eq. (7), is close to 0.2μs even in the worst case, according to 100 runs of *Monte Carlo* simulation results (Fig. 6). Moreover, the time interval will be less than 0.2μs with superior matching of the comparator's transistors which can be obtained through careful layout design. This means the time error ratio between T_{ref} and T_{int} is about 0.6% as the reference frequency is nearly 32.7K. According to the analysis in the subsection *A* of Section III, it is revealed that the intrinsic error induced by process variation is around ±60%. In order to achieve a resolution of 0.2%, a 9-bits counter is implemented to control the compensating capacitor, which is driven by the pulse generated by the comparator. The calibration loop is shut off when the output frequency becomes stable. Based on the small delay time variation of the comparator, a process insensitive criterion is acquired.

IV. Simulation Results

The proposed oscillator with auto-calibration was implemented in UMC 0.18μm 1P6M standard process. Figure 6 shows the operation frequency of the relaxation oscillator without auto-calibration (100 runs of *Monte Carlo* simulation

at room temperature). The mean value and standard deviation are 46.16 kHz and 9.48 kHz, respectively, with a 3σ inaccuracy of 20.5% as shown in Fig. 7. The oscillator operates with a supply voltage of 0.7V and the consumed power is 85.3nW.

The output frequency of the implemented relaxation oscillator with auto-calibration is shown in Fig. 8. The mean value and standard deviation is calculated to be 32.67 kHz and 445 Hz, respectively, with the process sensitivity (σ/μ) of 1.36%. This is a little bit larger than the theoretical analysis due to the additional time step error as mentioned in the subsection C of Section II. Table I shows the performance of our implementation and its comparison with the previously reported implementations. The phase noise of the proposed oscillator at offset frequency 1 kHz and 10 kHz are -62dBc/Hz and -86dBc/Hz, respectively. Tradeoff exists between the power consumption and relative process sensitivity in the comparator design.

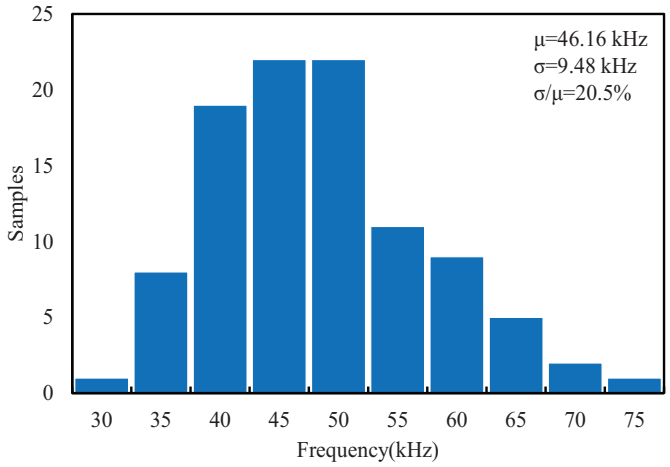

Fig. 7. Histogram of the original frequency for 100 runs of *Monte Carlo* simulation.

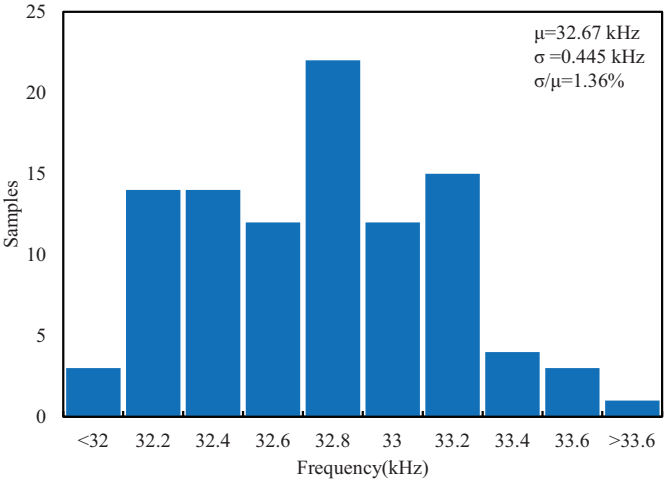

Fig. 8. Histogram of the calibrated frequency for 100 runs of *Monte Carlo* simulation.

TABLE I. PERFORMANCE COMPARISON

Ref.	[3][a]	[4][b]	[5][a]	This work[b]
Process	0.18μm CMOS	0.35μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply Voltage (V)	1.8	1	1~1.8	1
Frequency	31.25kHz	80 kHz	32.55 kHz	32.67 kHz
Power dissipation	0.36 μW	1.14 μW	0.47 μW	0.085μW[c] 0.19 μW[d]
Process sensitivity (σ/μ)	1.52% with calibration, 200 samples	11.85% without calibration	1.39% without calibration, 20 samples (same wafer)	1.36% with on-chip calibration
Area	0.0162 mm^2	0.24mm^2	0.105 mm^2	0.097mm^2

a-Measurement results. b-Simulation results. c-Oscillator Only d-Whole system

V. CONCLUSION

A process insensitive low-power relaxation oscillator with auto-calibration is proposed in this work. A process sensitivity of 1.36% is achieved by adopting the automatic sensing architecture and adjusting the compensating capacitor. Our proposed implementation is suitable for a wide range of wireless sensing network applications, where the power consumption are of utmost importance.

ACKNOWLEDGMENT

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